What is claimed is:

1. A synchronous signal/active signal restoring apparatus comprising:

an optical signal receiving unit for receiving an optical signal through an optical fiber from a source device;

a serial/parallel converter for converting a serial data of the optical signal received from the optical signal receiver into a parallel data;

a decoder for converting the 10 bit parallel data outputted from the serial/parallel converter into an 8 bit parallel data;

a first image signal processor for separating an image signal, a header and a tail from an image signal packet among output signals decoded from the decoder, and recognizing resolution information of the image signal through the image signal characteristic packet;

a first clock signal generator for generating a clock signal with a predetermined frequency according to the resolution information recognized by the first image signal processor;

a horizontal active signal/synchronous signal restoring unit for receiving the header, the tail and the resolution information from the first image signal processor, and restoring horizontal synchronous signal/active signal;

a vertical active signal/synchronous signal restoring unit for receiving the header and the resolution information from the first image signal processor and the horizontal synchronous signal from the horizontal active signal/synchronous signal generator, and restoring a vertical synchronous signal/active signal; and

an image signal outputting unit for receiving the separated image signal

from the first image signal processor, and outputting an image signal according to the horizontal active signal restored in the horizontal active signal/synchronous restoring unit.

2. The apparatus of claim 1, wherein the first image signal processor counts the number of active headers, and recognizes resolution information by using the counted number of active headers.

3. The apparatus of claim 1, wherein the resolution information is recognized as the number of active headers consecutive in the image signal packet.

4. The apparatus of claim 1, wherein the horizontal active signal/synchronous signal restoring unit generates a horizontal active signal by being synchronized with the clock signal according to the header and the tail inputted from the first image signal processor, and generates the horizontal synchronous signal by using the horizontal active signal, the resolution information and the clock signal.

5. The apparatus of claim 1, wherein the vertical active signal/synchronous signal restoring unit judges whether the header outputted from the first image signal processor is a blanking header or an active header, generates a vertical active signal according to the judged type of the header, and generates a vertical synchronous signal by using the vertical active signal, the resolution information and the clock signal.

6. The apparatus of claim 1, wherein the image signal outputting unit receives the horizontal active generated by the horizontal active signal/synchronous signal restoring unit, the image signal outputted from the first image signal processor, and the clock signal generated by the first clock generator, and outputs an image signal according to the clock signal in the active interval of the horizontal active signal

7. The apparatus of claim 1, wherein the horizontal active signal/synchronous signal restoring unit comprises:

an image signal reception recognizing unit for recognizing reception of the image signal through the header and the tail separated in the first image signal processor;

a horizontal active signal/synchronous signal controller for controlling generation of the horizontal active signal and counting predetermined number of clock signals according to the resolution information on the basis of the horizontal active signal, to thereby control generation of a horizontal synchronous signal; and

a horizontal active signal/synchronous signal generator for generating a horizontal active signal and a horizontal synchronous signal under the control of the horizontal active signal/synchronous signal controller.

8. The apparatus of claim 7, wherein the horizontal active signal/synchronous signal controller judges resolution of the image signal by the resolution information inputted from the first image signal processor, counts clock signals from a position of a tail at a time point when the image signal is not received yet, and controls the horizontal active signal/synchronous signal

generator 420 according to the counted number of clock signals according to the resolution.

9. The apparatus of claim 1, wherein the vertical active signal/synchronous signal restoring unit comprises:

a header discriminator for discriminating whether a header inputted from the image signal processor is a blanking header or an active header;

a vertical active signal/synchronous signal controller for controlling generation of a vertical active signal according to an output signal of the header discriminator and counting predetermined number of horizontal synchronous signals according to resolution information on the basis of the vertical active signal, to thereby control generation of the vertical synchronous signal; and

a vertical active signal/synchronous signal generator for generating a vertical active signal and a vertical synchronous signal under the control of the vertical active signal/synchronous signal controller.

10. The apparatus of claim 9, wherein the vertical active signal/synchronous signal controller generates a vertical active signal which is active during an interval where the active header is continuously recognized and is blank during an interval where the blanking header is continuously recognized.

11. An active signal/synchronous signal restoring apparatus comprising:

an optical signal receiver for receiving an optical signal through an optical fiber from a source device;

a serial/parallel converter for converting a serial data of the optical signal received from the optical signal receiver into a parallel data;

a decoder for converting a 10 bit parallel data outputted from the serial/parallel converter into an 8-bit parallel data;

a second image signal processor for separating an image signal, a header and a tail from an image signal packet among output signals decoded from the decoder, and recognizing resolution information of the image signal through the image signal characteristic packet;

a second clock signal generator for generating a clock signal with a predetermined frequency according to the resolution information recognized by the second image signal processor;

a counter for counting a clock signal generated by the second clock signal generator;

a maximum count value controller for setting a maximum count value according to the resolution information recognized by the second image signal processor, and variably setting the maximum count value depending on whether the counter counts a pre-set maximum count value within a period of the header recognized by the second image signal processor; and

a horizontal active signal/synchronous signal generator for generating a horizontal active signal and a horizontal synchronous signal as the counter counts a pre-set value according to the resolution information recognized by the second image signal processor.

12. The apparatus of claim 11, wherein the resolution information is recognized by the number of active headers successive in the image signal packet.

13. The apparatus of claim 11, wherein the maximum count value controller sets the counter to repeatedly count a maximum count value whenever a pre-set number of headers are inputted, and variably sets the maximum count value according to the repeated count result.

14. The apparatus of claim 13, wherein, before the header is inputted, if the maximum count completion number of the counter is greater than the pre-set value, the maximum count value controller adds 1 to the maximum count value of the counter, whereas if the header input number is greater than the pre-set value, the maximum count value controller subtracts 1 from the maximum count value of the counter.

15. An active signal/synchronous signal restoring method comprising:

a first step of setting a maximum count value of a counter according to resolution information recognized by an image signal processor;

a second step of judging whether a header has been inputted from the image signal processor;

a third step of resetting the counter and adding 1 to a clock signal count number (N) of the counter if a header is inputted from the image signal processor;

a fourth step of judging whether the counter has counted the pre-set maximum count value;

a fifth step of adding 1 to the maximum count completion number (A) if the counter has counted the pre-set maximum count value;

a sixth step of judging whether the clock signal count number (N0 is greater than a pre-set value;

a seventh step of judging whether the count number (A) of the maximum count value of the counter before the header is inputted is greater than the pre-set value, if the clock signal count number (N) is greater than the pre-set value; and

an eighth step of adding 1 to the maximum count value and setting the value at the counter, if the count number (A) is greater than the pre-set value.

16. The method of claim 15 further comprising:

judging whether a header has been inputted from a second image signal processor, if the counter has not counted the pre-set maximum count value.

17. The method of claim 15, wherein, if the clock signal count number (N) is not greater than the pre-set value, it returns to the second step to repeatedly perform the operation that a header is inputted, the counter is reset to count a clock signal again, and 1 is added to the clock signal count number (N).

18. The method of claim 15, wherein, if the counter has not counted the pre-set maximum count value, that is, if a header is inputted from the second image signal processor before the counter counts the maximum count value, 1 is added to the header input number (B), and it is judged whether the clock signal count number (N) is greater than the pre-set value, and if the clock signal count number (N) is not greater than the pre-set value, the operation that the counter is reset to count clock signals and 1 is added to the clock signal count number (N) is repeatedly performed.

19. The method of claim 15, wherein if the count number (a) is not

greater than the pre-set value, it is judged whether the header input number (B) is greater than the pre-set value before the counter counts the maximum count value, and if the header input number (B) is greater than the pre-set value, 1 is subtracted from the maximum count value and set in the counter.